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# FQD3P50

## P-Channel QFET<sup>®</sup> MOSFET

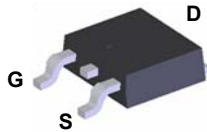
- 500 V, - 2.1 A, 4.9 Ω

### Description

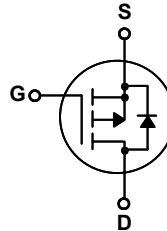
This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor<sup>®</sup>'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- - 2.1 A, - 500 V,  $R_{DS(on)} = 4.9 \Omega$  (Max.) @  $V_{GS} = -10 V$ ,  $I_D = -1.05 A$
- Low Gate Charge (Typ. 18 nC)
- Low  $C_{rss}$  (Typ. 9.5 pF)
- 100% Avalanche Tested



**D-PAK  
(TO252)**



### Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	FQD3P50	Unit
$V_{DSS}$	Drain-Source Voltage	-500	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ ) - Continuous ( $T_C = 100^\circ C$ )	-2.1	A
		-1.33	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	-8.4	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	250	mJ
$I_{AR}$	Avalanche Current (Note 1)	-2.1	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-4.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ C$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ C$ ) - Derate above $25^\circ C$	50	W
		0.4	W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ C$

### Thermal Characteristics

Symbol	Parameter	FQD3P50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.5	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max. *	50	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	110	$^\circ C/W$

\* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.42	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -500\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
		$V_{DS} = -400\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

## On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -1.05\text{ A}$	--	3.9	4.9	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -50\text{ V}, I_D = -1.05\text{ A}$	--	2.1	--	S

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	510	660	pF
$C_{oss}$	Output Capacitance		--	70	90	pF
$C_{rss}$	Reverse Transfer Capacitance		--	9.5	12	pF

## Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -250\text{ V}, I_D = -2.7\text{ A},$ $R_G = 25\ \Omega$	--	12	35	ns
$t_r$	Turn-On Rise Time		--	56	120	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	80	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	45	100
$Q_g$	Total Gate Charge	$V_{DS} = -400\text{ V}, I_D = -2.7\text{ A},$ $V_{GS} = -10\text{ V}$	--	18	23	nC
$Q_{gs}$	Gate-Source Charge		--	3.6	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	9.2	--

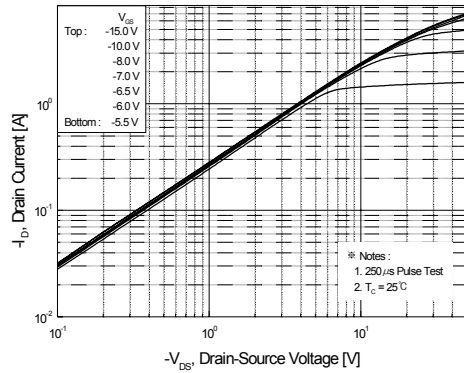
## Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	-2.1	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-8.4	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.1\text{ A}$	--	--	-5.0	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -2.7\text{ A},$	--	270	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$	--	1.5	--	$\mu\text{C}$

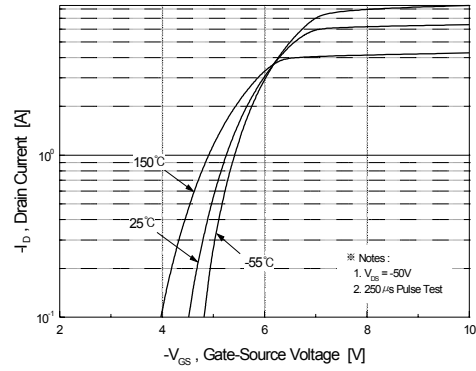
### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 102\text{mH}, I_{AS} = -2.1\text{ A}, V_{DD} = -50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq -2.7\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature

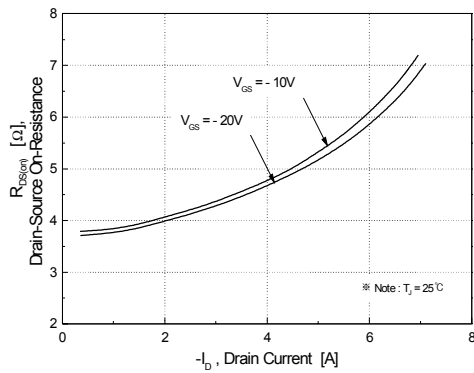
## Typical Characteristics



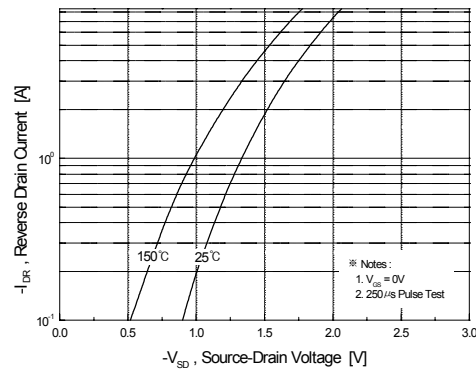
**Figure 1. On-Region Characteristics**



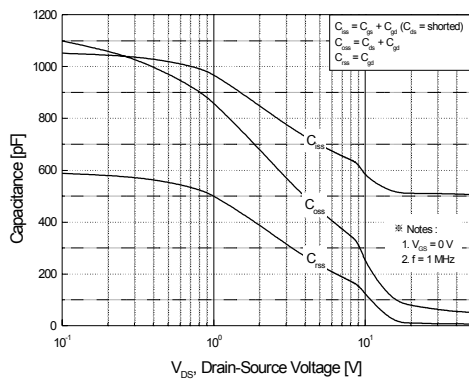
**Figure 2. Transfer Characteristics**



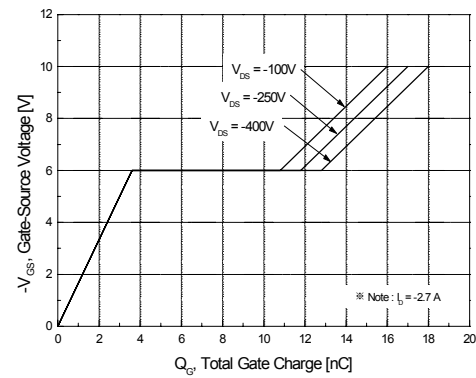
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

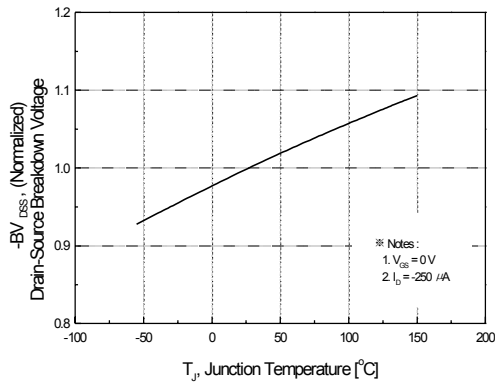


**Figure 5. Capacitance Characteristics**

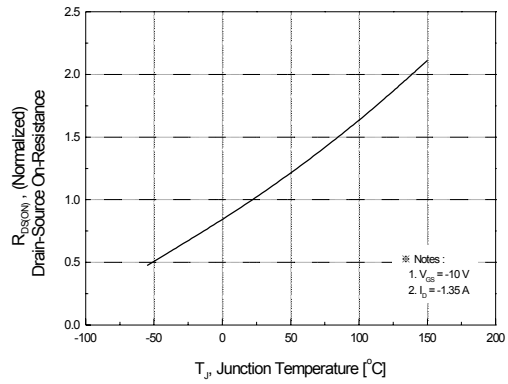


**Figure 6. Gate Charge Characteristics**

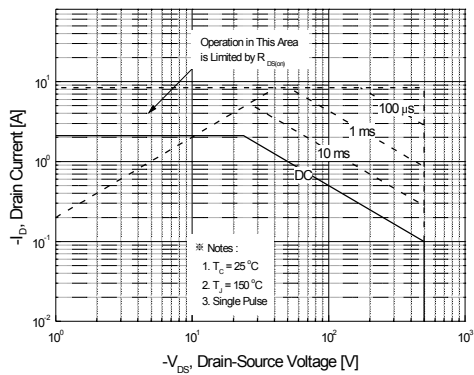
**Typical Characteristics** (Continued)



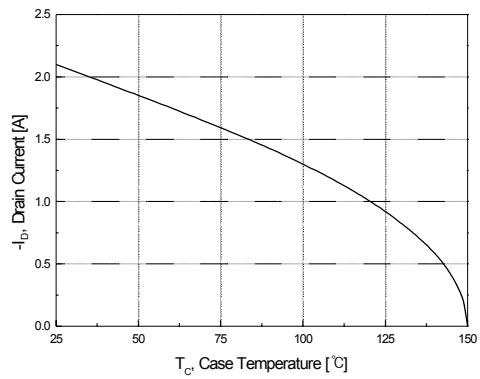
**Figure 7. Breakdown Voltage Variation vs. Temperature**



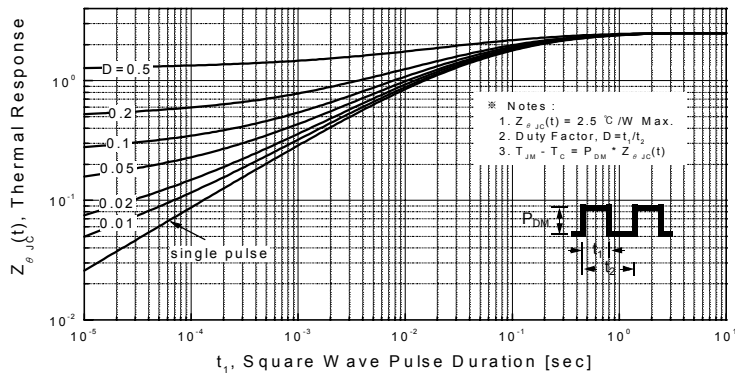
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

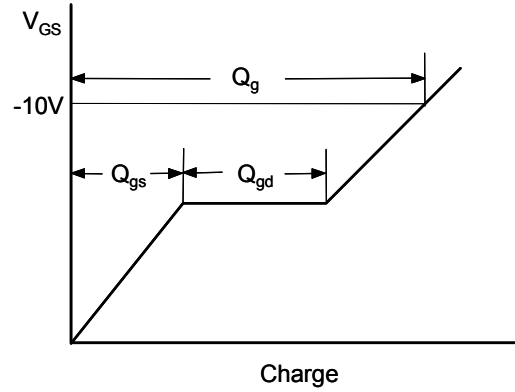
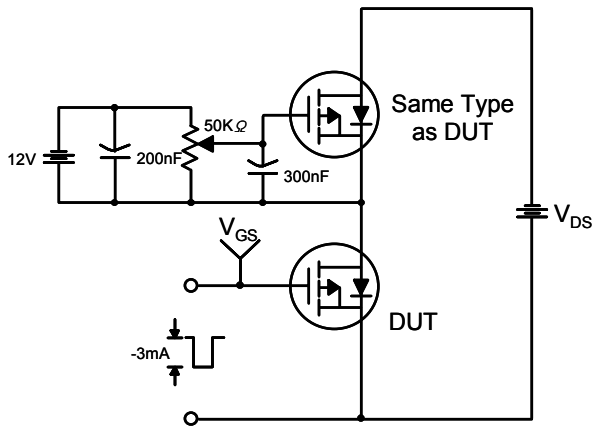


**Figure 10. Maximum Drain Current vs. Case Temperature**

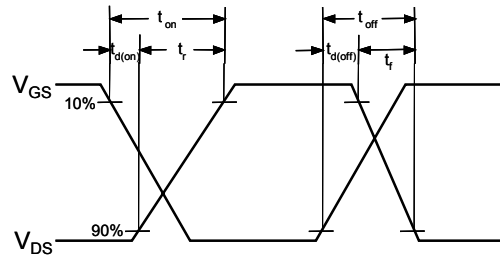
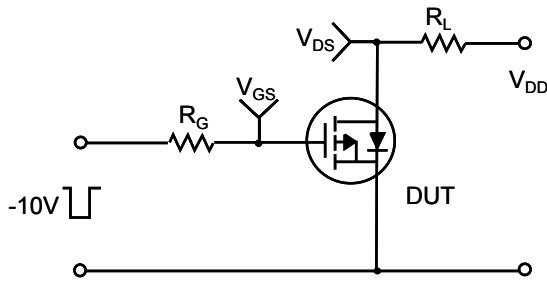


**Figure 11. Transient Thermal Response Curve**

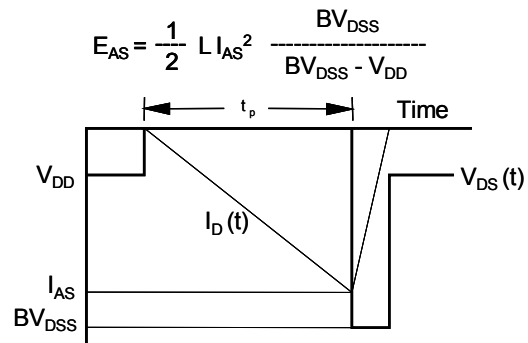
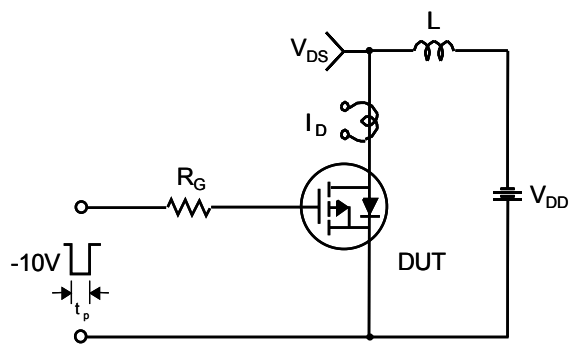
**Gate Charge Test Circuit & Waveform**



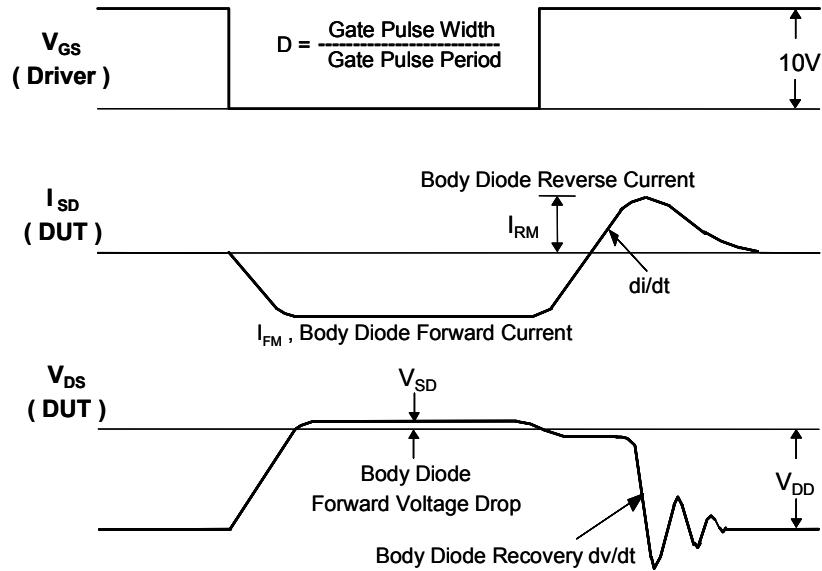
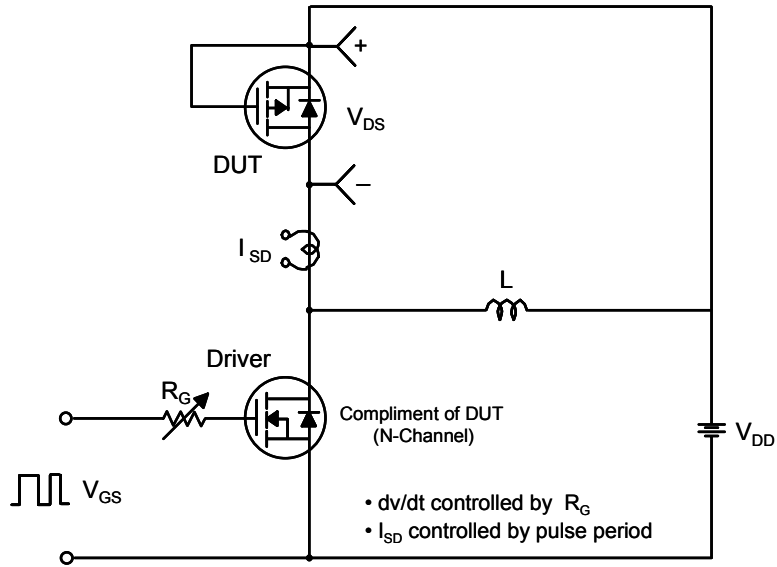
**Resistive Switching Test Circuit & Waveforms**

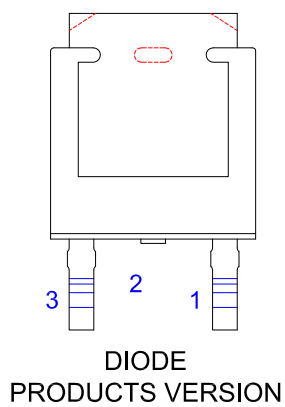


**Unclamped Inductive Switching Test Circuit & Waveforms**



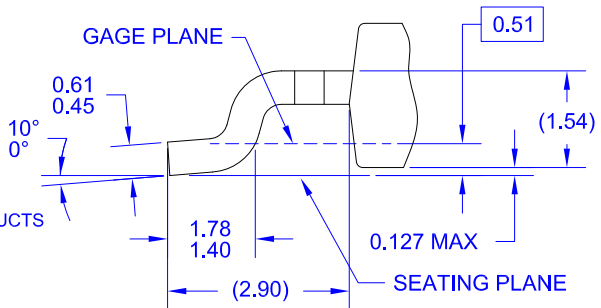
Peak Diode Recovery dv/dt Test Circuit & Waveforms





NOTES: UNLESS OTHERWISE SPECIFIED

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- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
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